

10/814, 943

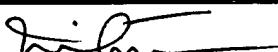
Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 001207.P011	Application Number: Not yet assigned
		First Named Inventor: Peter M. Pani	
		Filing Date: Herewith	

U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Code ²	Kind (If known)			
W		4,912,342		Wong, et al.	3/1990	
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W/ln	Re 34,363			Freeman	8/1993	
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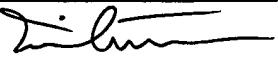
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JKW		5,243,238		Kean	9/7/93	
1		5,256,918		Suzuki	10/1993	
		5,260,610		Pederson, et al.	11/9/93	
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		5,296,759		Sutherland, et al.	3/22/94	
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<i>Yan</i>		6,016,063		Trimberger	1/2000	
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		Office ³	Number ⁴	Kind Code ⁵ (If known)				
<i>OT</i>		EPO	0415542		Advanced Micro Devices, Inc.	3/6/91		
		EPO	0630115A2		Pilkington Micro-Electronics Limited	6/1/94		
		PCT	9410754		Xilinx, Inc.	5/11/94		
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		PCT	9504404		Advantage Logic, Inc.	2/9/95		
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		PCT	9428475		Regents of the University of California	12/8/94		
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<i>OT</i>		UK	2295738		Altera Corporation	5/6/96		

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OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
<i>PM</i>		Altera Corporation Date Sheet, Flex EPF81188 12,000 Gate Programmable Logic Device, September 1992, Ver. 1, pp. 1-20.	
<i>PM</i>		ATMEL Field Programmable Arrays, AT 6000 Series, 1993, p. 1-16. Coprocessor Field Programmable Gate arrays AT 6000(LV) Series, 10/99, Page 1-27.	
<i>PM</i>		BRITTON, et al., "Optimized Reconfigurable Cell Array Architecture for High-Performance Field Programmable Gate Arrays," Proceedings of the IEEE 1993 Custom Integrated Circuits Conference, 1993, pp. 7.2.1. - 7.2.5. 3/93	
<i>PM</i>		BUFFOLI, E., et al., "Dynamically Reconfigurable Devices Used to Implement a Self-Tuning, High Performances PID Controller," 1989 IEEE, pp., 107-112. 8/89	
<i>PM</i>		BURSKY, D., "Fine-Grain FPGA Architecture Uses Four Levels of Configuration Hierarchy," 2328 Electronic Design, 41, No. 20, Cleveland, OH, October 1, 1993, pp. 33-34.	
<i>PM</i>		Cliff, et al., "A Dual Granularity and Globally Interconnected Architecture for a Programmable Logic Device", IEEE '93 pp. 7.3.1-7.3.5. 3/93	
<i>PM</i>		DEVADES, S., et al., "Boolean Decomposition of Programmable Logic Arrays," IEEE 1988, pp. 2.5.1 - 2.5.5. 1/88	
<i>PM</i>		F. Zlotnick, P. Butler, W. Li, D. Tang, "A High Performance Fine-Grained Approach to SRAM Based FPGAs", p. 321-326, Wescon September 28-30, 1993.	
<i>PM</i>		LIU, D.L., et al., "Design of Large Embedded CMOS PLA's for Built-In Self-test," IEEE Transactions on Computed-Aided Design, Vol. 7, No. 1, January 1988, pp. 50-53.	
<i>PM</i>		Minnick, R.C., "A Survey of Microcellular Research", vol. 14, no. 2, 4/1967, pp. 203-241.	

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Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
UTan		Motorola Project Brief, "MPA10xx Field Programmable Gate Arrays," September 27, 1993, 2 pages.	
UTan		Robert H. Krambeck, "ORCA: A High Performance, Easy to Use SRAM Based Architecture", p. 310-320, Wescon September 28-30, 1993.	
UTan		SHOUP, R. G., "Programmable Cellular Logic Arrays," Abstract, Ph.D. Dissertation, Carnegie Mellon University, Pittsburgh, PA, March 1970, (partial) pp. ii-121.	
UTan		Sinan Kaptanoglu, Greg Bakker, Arun Kundu, Ivan Corneillet, Ben Ting, "A New High Density and Very Low Cost Reprogrammable FPGA Architecture", 10 pages, Actel Corporation. <u>No date</u> .	
UTan		SPANDORFER, L.M., "Synthesis of Logic Functions on an Array of Integrated Circuits," Contract No. AF 19 (628) 2907, Project No. 4645, Task No. 464504, Final Report, November 30, 1965.	
UTan		SUN, Y., et al., "An Area Minimizer for Floorplans with L-Shaped Regions," 1992 International Conference on Computer Design, 1992 IEEE, pp. 383-386. <u>4/92</u>	
UTan		VIDAL, J. J., "Implementing Neural Nets with Programmable Logic," IEEE Transactions on Acoustic, Speech, and Signal Processing, Vol. 36, No. 7, July 1988, pp. 1180-1190.	
UTan		Wang, P. et al. IEEE, "A High Performance FPGA with Hierarchical Interconnection Structure", pp. 239-242 (May 30, 1994).	
		Xilinx, "The Programmable Gate Array Data Book", 1992. <u>only table of contents Scanned</u> . <u>UTan</u>	

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